EEL4744

Menu

- What's important?
  - > Architecture Issues
  - > Bus Widths
  - > Non-volatile Memory
  - > Data Memory
- Components of previous processors
- UF Development Board (show & tell)
- Some XMEGA Specs

See examples on web-site:
doc8331(XMEGA AU Manual)
doc8385(128A1U Manual)
µPAD Schematic(s)

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What's important?

- Architectural Issues
  - > Instruction set
  - > Data path widths
  - > Timing and clock cycles
  - > Is buffering required?
  - > Power consumption
  - > Packaging
  - > Timers
  - > I/O ports
  - > A/D, D/A
  - > Power up/down
  - > Battery backup
  - > Family support
  - > Documentation
  - > Part availability

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What's important?

- Bus Widths
  - > Early µP had 4-bit operands.
  - > 68HC11/2 has 8-bit operands and some 16-bit operands. 68HC11 is an 8-bit µC. The 68HC12 is an 8/16-bit µC. Instructions that deal with 16-bit operands take 2 cycles to transfer the 16 bits over the data bus.
  - > The 68HC11/68HC12 (68HC912B32) 16-bit address bus gives access to 2^{16} = 64K addresses.
  - > The TI TMS320F28335 DSC has a 32-bit data bus, but can also be used in a 16-bit data bus mode
  - > **Our XMEGA** is a 8/16-bit processor
    - – 8-bit data
    - – 16-bit addresses registers and 24-bit addresses

3

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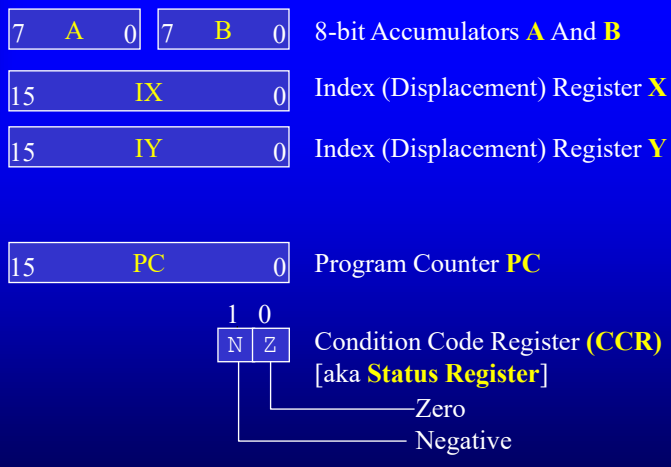
Programming Model for GCPU



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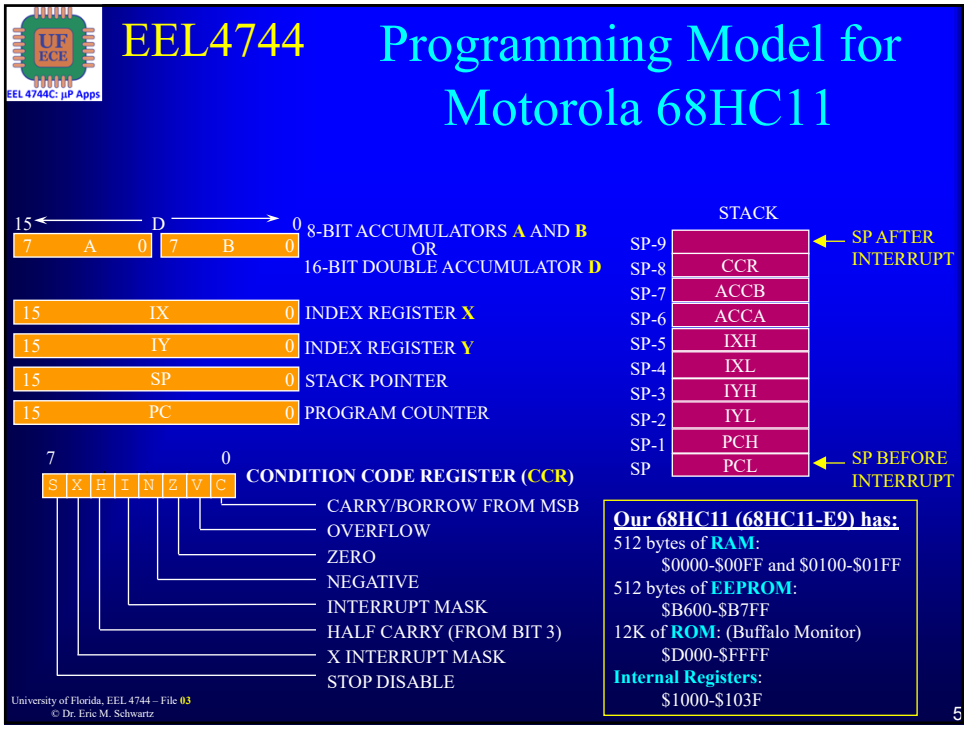
EEL4744
Programming Model for Motorola 68HC11
EEL 4744C: µP Apps
15 D 0
7 A 0
7 B 0
8-BIT ACCUMULATORS A AND B
OR
16-BIT DOUBLE ACCUMULATOR D
15 IX 0
INDEX REGISTER X
15 IY 0
INDEX REGISTER Y
15 SP 0
STACK POINTER
15 PC 0
PROGRAM COUNTER
7 0
S X H I N Z V C
CONDITION CODE REGISTER (CCR)
CARRY/BORROW FROM MSB
OVERFLOW
ZERO
NEGATIVE
INTERRUPT MASK
HALF CARRY (FROM BIT 3)
X INTERRUPT MASK
STOP DISABLE
STACK
SP-9
SP-8 CCR
SP-7 ACCB
SP-6 ACCA
SP-5 IXH
SP-4 IXL
SP-3 IYH
SP-2 IYL
SP-1 PCH
SP PCL
SP AFTER INTERRUPT
SP BEFORE INTERRUPT
Our 68HC11 (68HC11-E9) has:
512 bytes of RAM:
$0000-$00FF and $0100-$01FF
512 bytes of EEPROM:
$B600-$B7FF
12K of ROM: (Buffalo Monitor)
$D000-$FFFF
Internal Registers:
$1000-$103F
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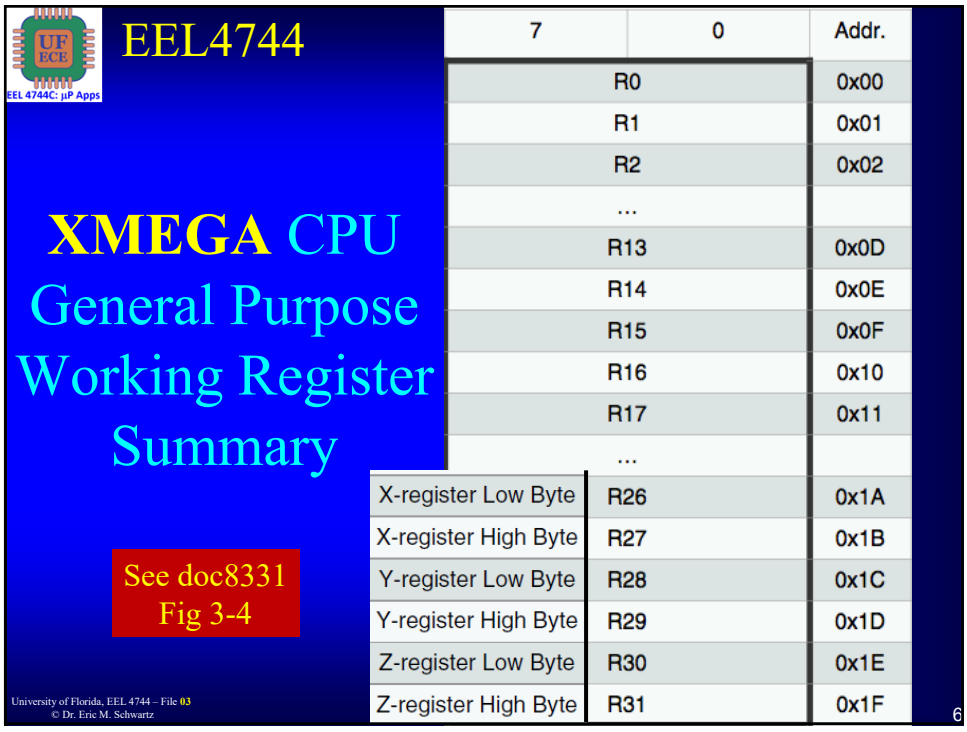
EEL4744
EEL 4744C: µP Apps
XMEGA CPU General Purpose Working Register Summary
See doc8331 Fig 3-4
7 0 Addr.
R0 0x00
R1 0x01
R2 0x02
...
R13 0x0D
R14 0x0E
R15 0x0F
R16 0x10
R17 0x11
...
X-register Low Byte R26 0x1A
X-register High Byte R27 0x1B
Y-register Low Byte R28 0x1C
Y-register High Byte R29 0x1D
Z-register Low Byte R30 0x1E
Z-register High Byte R31 0x1F
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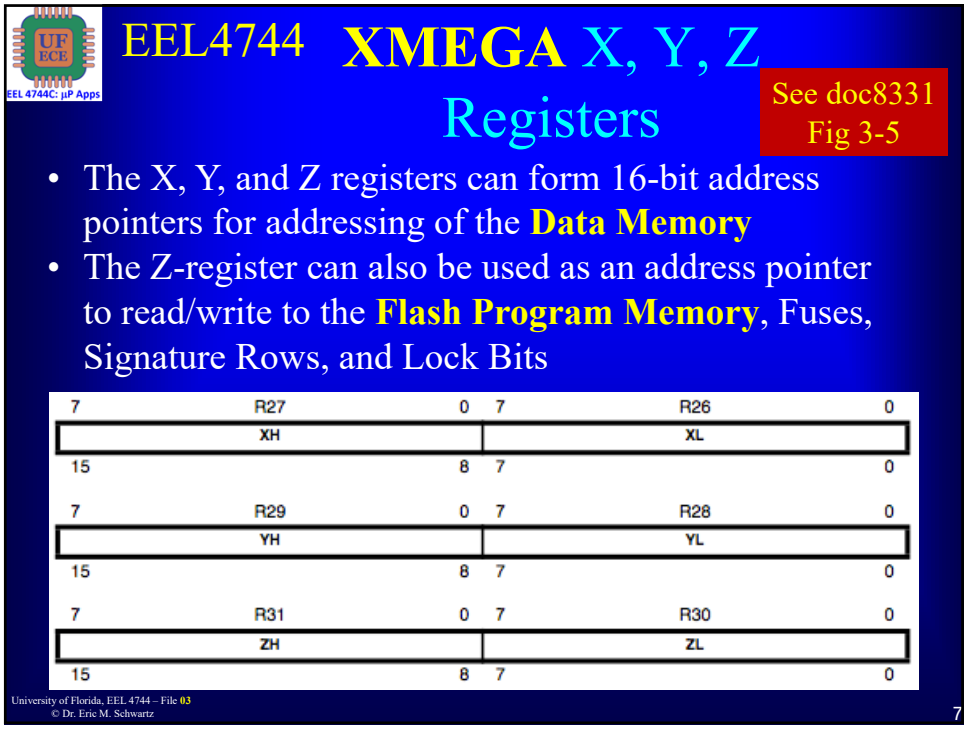
EEL4744
XMEGA X, Y, Z Registers
See doc8331 Fig 3-5
• The X, Y, and Z registers can form 16-bit address pointers for addressing of the Data Memory
• The Z-register can also be used as an address pointer to read/write to the Flash Program Memory, Fuses, Signature Rows, and Lock Bits
7 R27 0 7 R26 0
XH XL
15 8 7 0
7 R29 0 7 R28 0
YH YL
15 8 7 0
7 R31 0 7 R30 0
ZH ZL
15 8 7 0
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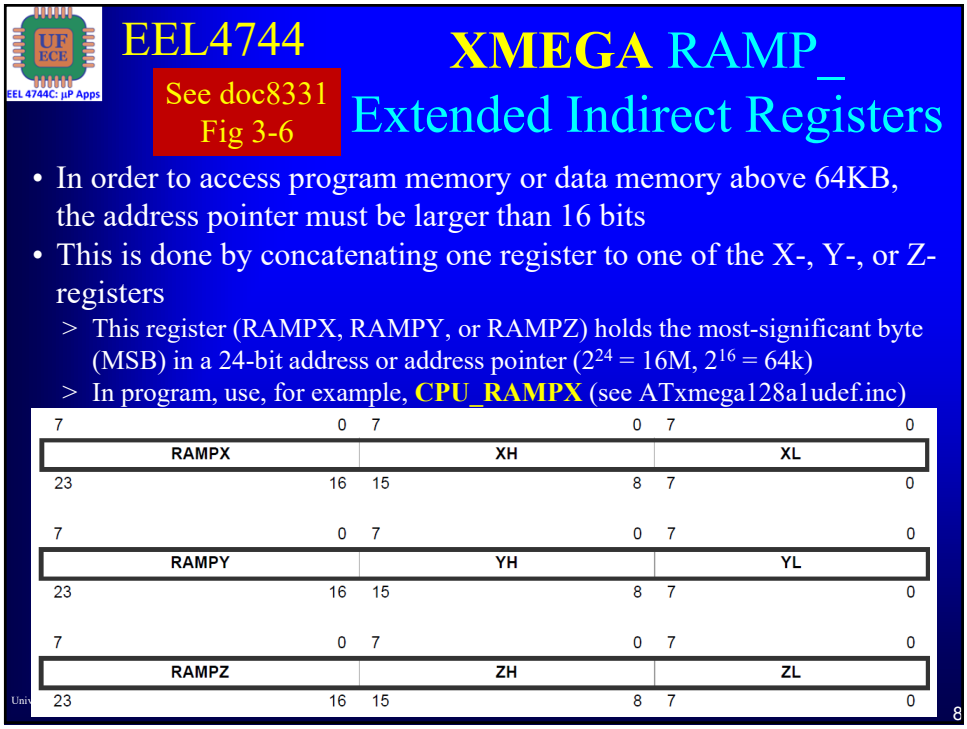
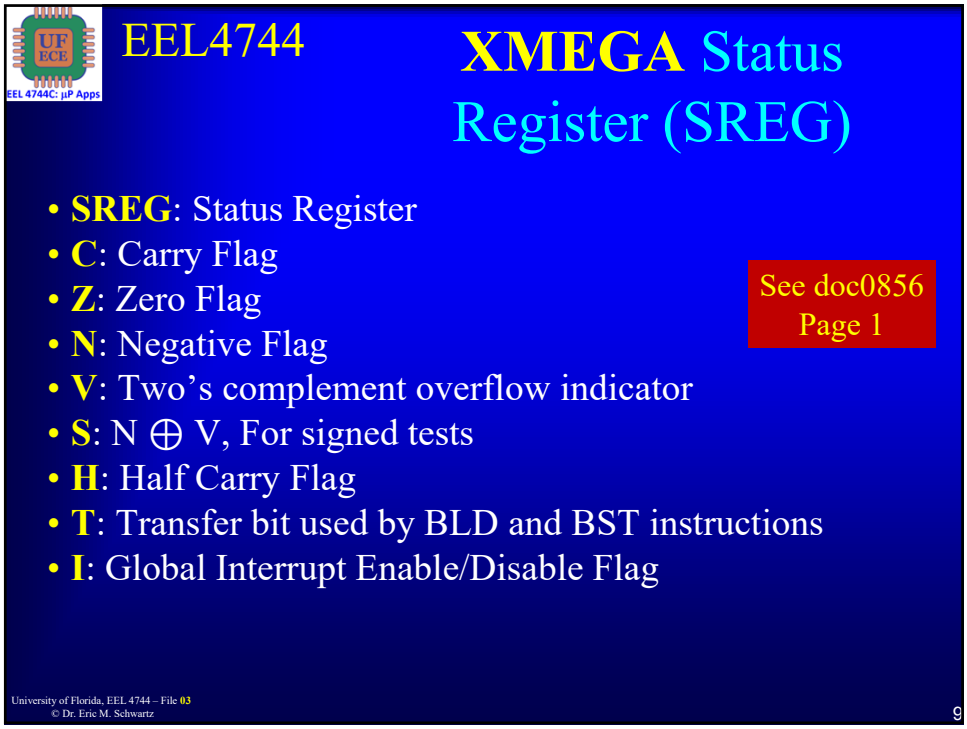

EEL4744
See doc8331 Fig 3-6
XMEGA RAMP_ Extended Indirect Registers
• In order to access program memory or data memory above 64KB, the address pointer must be larger than 16 bits
• This is done by concatenating one register to one of the X-, Y-, or Z-registers
> This register (RAMPX, RAMPY, or RAMPZ) holds the most-significant byte (MSB) in a 24-bit address or address pointer (2^{24} = 16M, 2^{16} = 64k)
> In program, use, for example, CPU_RAMPX (see ATxmega128a1udef.inc)
7 0 7 0 7 0
RAMPX XH XL
23 16 15 8 7 0
7 0 7 0 7 0
RAMPY YH YL
23 16 15 8 7 0
7 0 7 0 7 0
RAMPZ ZH ZL
23 16 15 8 7 0
8

8


EEL4744
XMEGA Status Register (SREG)
• SREG: Status Register
• C: Carry Flag
• Z: Zero Flag
• N: Negative Flag
• V: Two's complement overflow indicator
• S: N ⊕ V, For signed tests
• H: Half Carry Flag
• T: Transfer bit used by BLD and BST instructions
• I: Global Interrupt Enable/Disable Flag
See doc0856 Page 1
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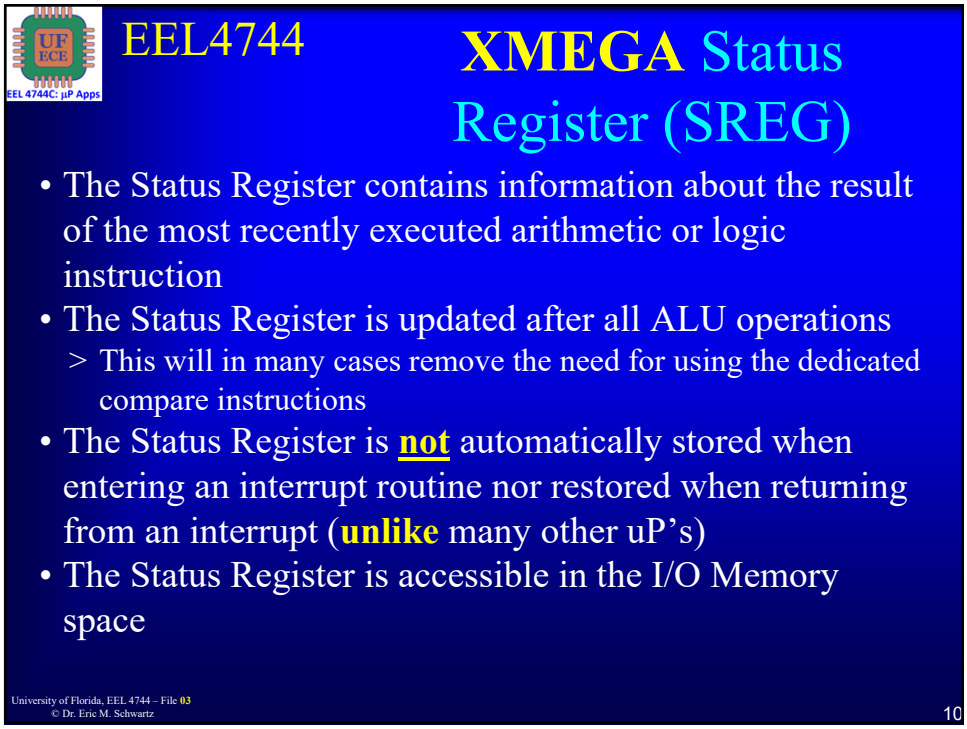
EEL4744
XMEGA Status Register (SREG)
• The Status Register contains information about the result of the most recently executed arithmetic or logic instruction
• The Status Register is updated after all ALU operations
> This will in many cases remove the need for using the dedicated compare instructions
• The Status Register is not automatically stored when entering an interrupt routine nor restored when returning from an interrupt (unlike many other uP's)
• The Status Register is accessible in the I/O Memory space
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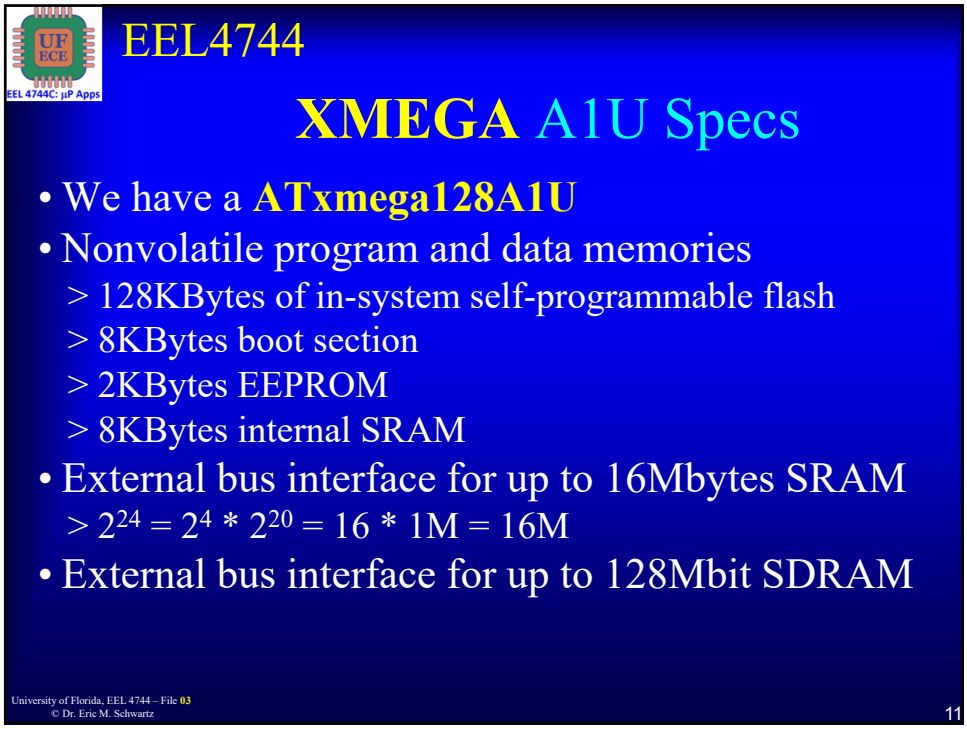
EEL4744
XMEGA A1U Specs
• We have a ATxmega128A1U
• Nonvolatile program and data memories
> 128KBytes of in-system self-programmable flash
> 8KBytes boot section
> 2KBytes EEPROM
> 8KBytes internal SRAM
• External bus interface for up to 16Mbytes SRAM
> 2^24 = 2^4 * 2^20 = 16 * 1M = 16M
• External bus interface for up to 128Mbit SDRAM
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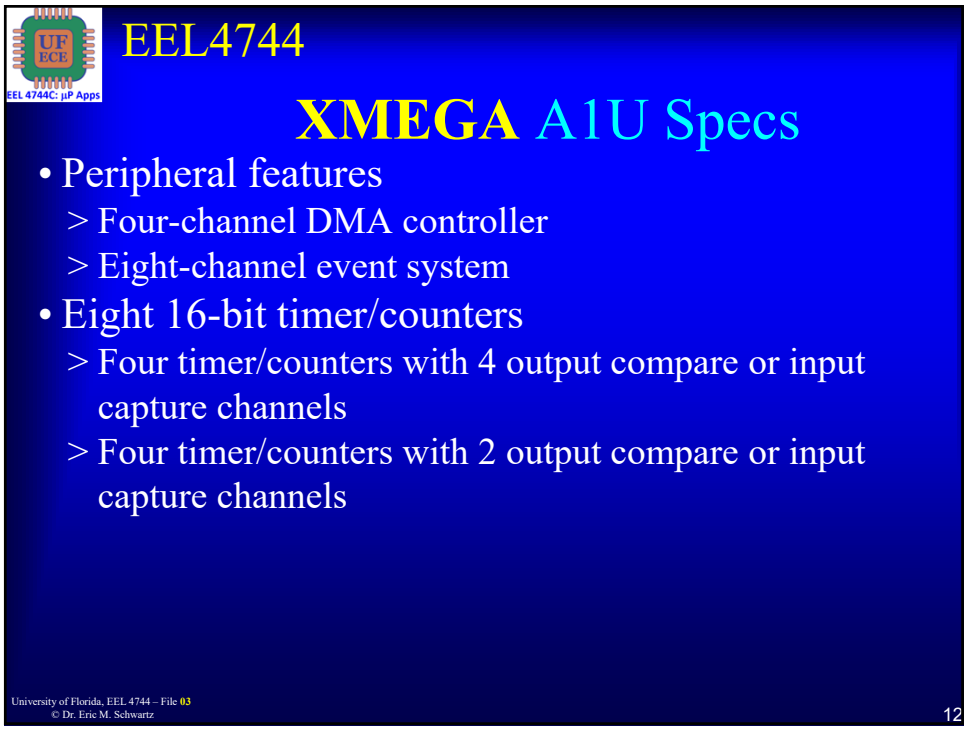
EEL4744
XMEGA A1U Specs
• Peripheral features
> Four-channel DMA controller
> Eight-channel event system
• Eight 16-bit timer/counters
> Four timer/counters with 4 output compare or input capture channels
> Four timer/counters with 2 output compare or input capture channels
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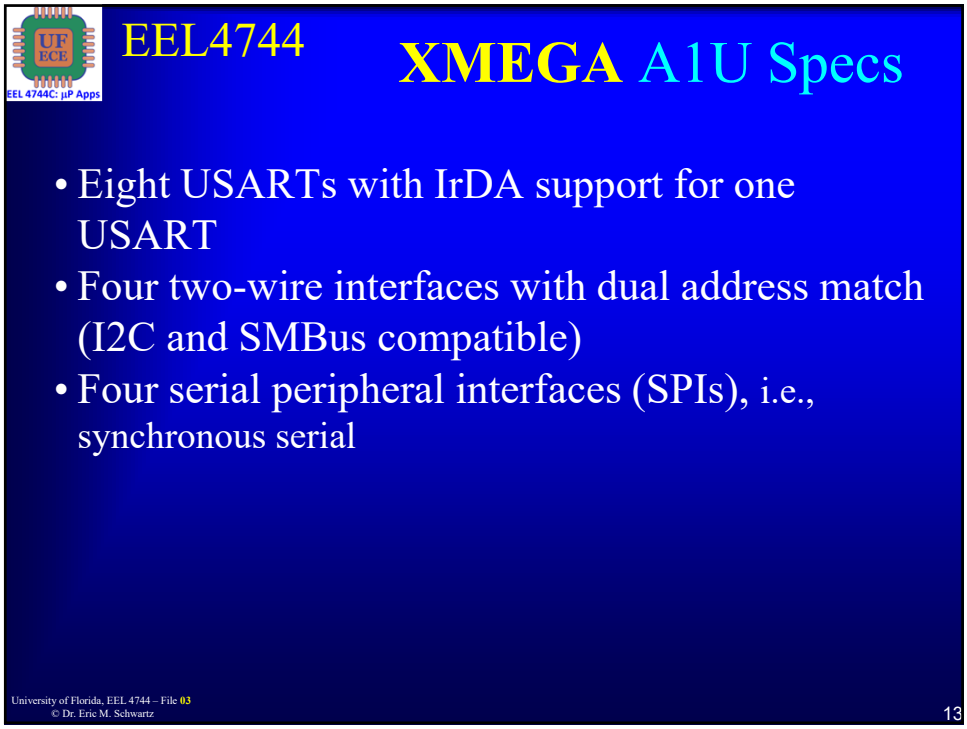
EEL4744
XMEGA A1U Specs
• Eight USARTs with IrDA support for one USART
• Four two-wire interfaces with dual address match (I2C and SMBus compatible)
• Four serial peripheral interfaces (SPIs), i.e., synchronous serial
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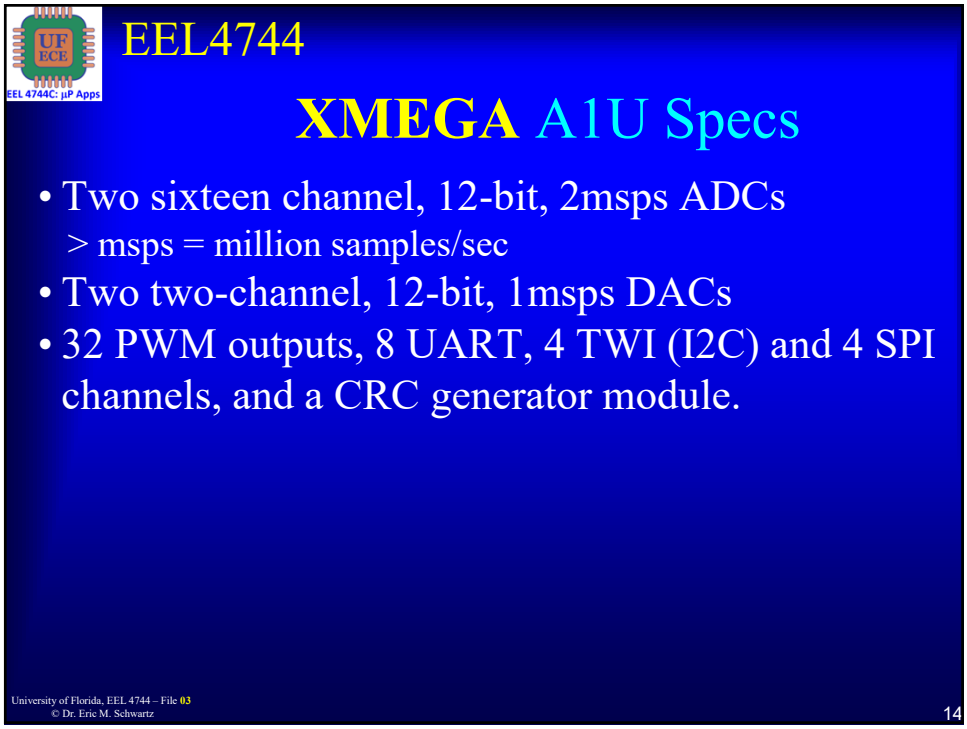
EEL4744
XMEGA A1U Specs
• Two sixteen channel, 12-bit, 2msps ADCs
> msps = million samples/sec
• Two two-channel, 12-bit, 1msps DACs
• 32 PWM outputs, 8 UART, 4 TWI (I2C) and 4 SPI channels, and a CRC generator module.
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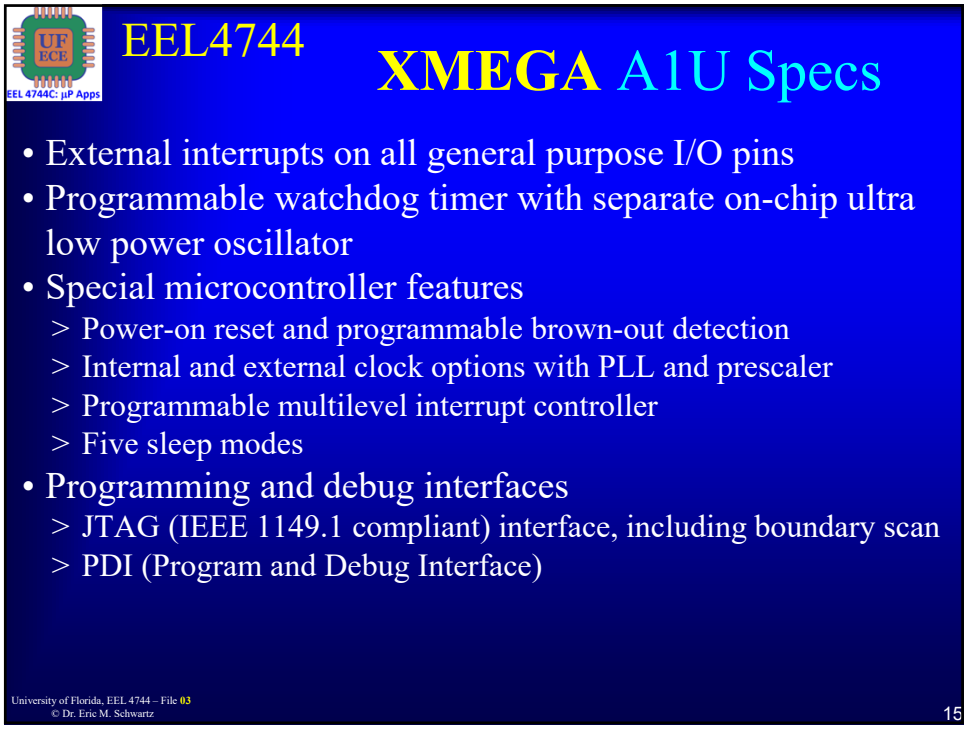
EEL4744
XMEGA A1U Specs
• External interrupts on all general purpose I/O pins
• Programmable watchdog timer with separate on-chip ultra low power oscillator
• Special microcontroller features
> Power-on reset and programmable brown-out detection
> Internal and external clock options with PLL and prescaler
> Programmable multilevel interrupt controller
> Five sleep modes
• Programming and debug interfaces
> JTAG (IEEE 1149.1 compliant) interface, including boundary scan
> PDI (Program and Debug Interface)
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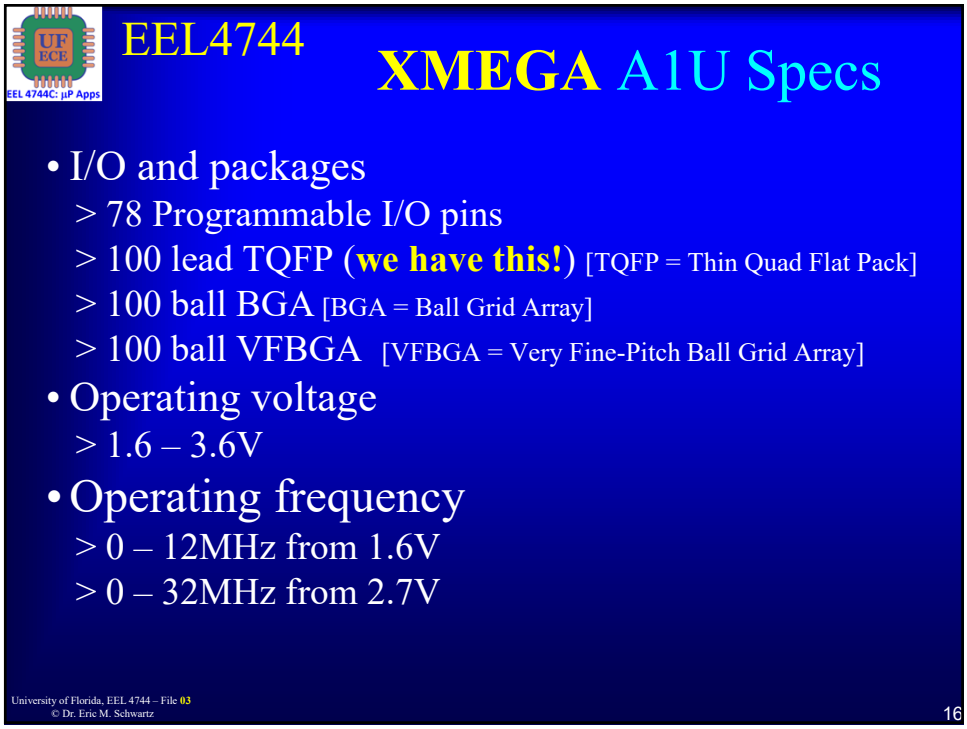
EEL4744
XMEGA A1U Specs
• I/O and packages
> 78 Programmable I/O pins
> 100 lead TQFP (we have this!) [TQFP = Thin Quad Flat Pack]
> 100 ball BGA [BGA = Ball Grid Array]
> 100 ball VFBGA [VFBGA = Very Fine-Pitch Ball Grid Array]
• Operating voltage
> 1.6 – 3.6V
• Operating frequency
> 0 – 12MHz from 1.6V
> 0 – 32MHz from 2.7V
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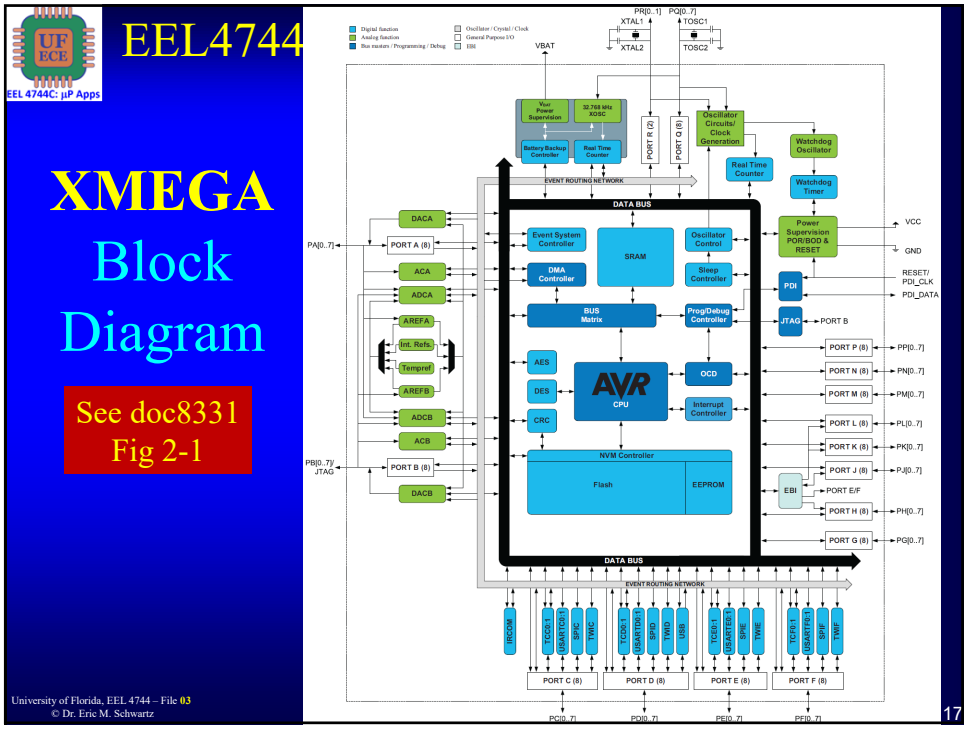
EEL4744
EEL 4744C: µP Apps
XMEGA
Block
Diagram
See doc8331
Fig 2-1
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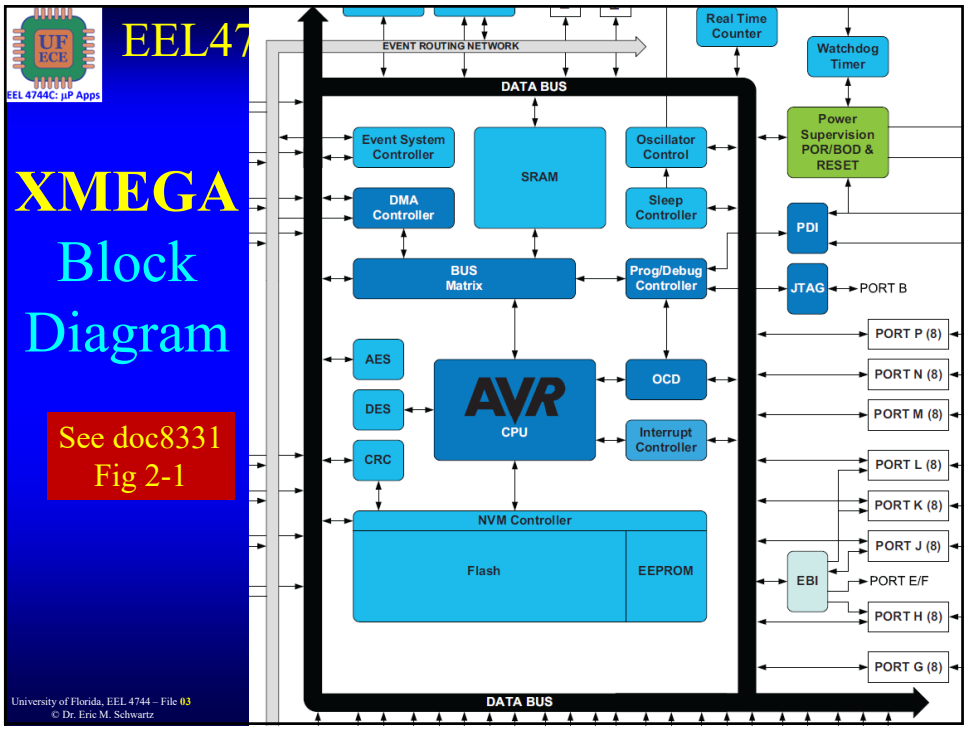
EEL47
EEL 4744C: µP Apps
XMEGA
Block
Diagram
See doc8331
Fig 2-1
EVENT ROUTING NETWORK
DATA BUS
Real Time Counter
Watchdog Timer
Event System Controller
SRAM
Oscillator Control
Power Supervision POR/BOD & RESET
DMA Controller
Sleep Controller
PDI
BUS Matrix
Prog/Debug Controller
JTAG
PORT B
AES
DES
CRC
AVR
CPU
OCD
Interrupt Controller
PORT P (8)
PORT N (8)
PORT M (8)
NVM Controller
Flash
EEPROM
PORT L (8)
PORT K (8)
PORT J (8)
EBI
PORT E/F
PORT H (8)
PORT G (8)
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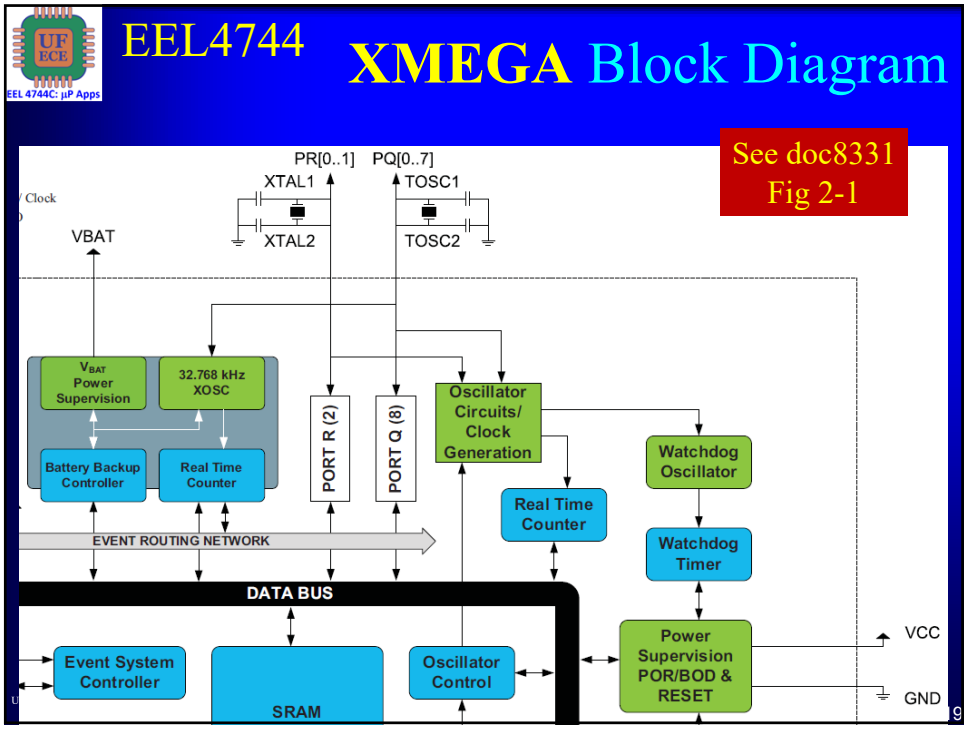
EEL4744
XMEGA Block Diagram
See doc8331
Fig 2-1
PR[0..1]
PQ[0..7]
XTAL1
XTAL2
TOSC1
TOSC2
Clock
VBAT
VBAT Power Supervision
32.768 kHz XOSC
Battery Backup Controller
Real Time Counter
PORT R (2)
PORT Q (8)
Oscillator Circuits/ Clock Generation
Watchdog Oscillator
Real Time Counter
Watchdog Timer
EVENT ROUTING NETWORK
DATA BUS
Event System Controller
SRAM
Oscillator Control
Power Supervision POR/BOD & RESET
VCC
GND

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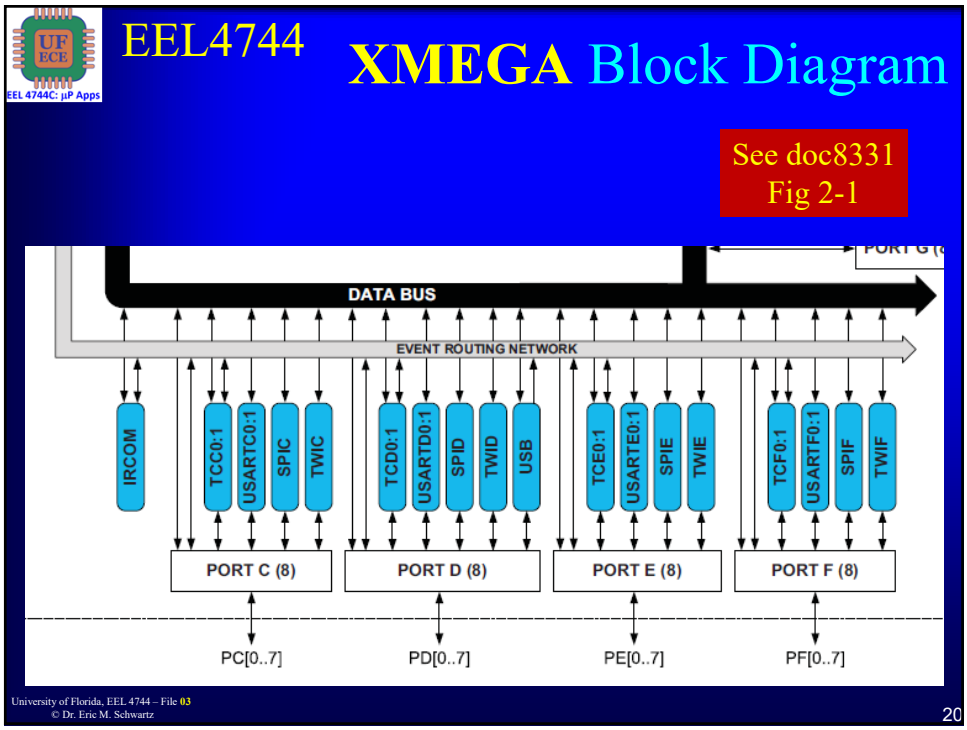
EEL4744
XMEGA Block Diagram
See doc8331
Fig 2-1
DATA BUS
EVENT ROUTING NETWORK
IRCOM
TCC0:1
USARTC0:1
SPIC
TWIC
TCD0:1
USARTD0:1
SPID
TWID
USB
TCE0:1
USARTE0:1
SPIE
TWIE
TCF0:1
USARTF0:1
SPIF
TWIF
PORT C (8)
PORT D (8)
PORT E (8)
PORT F (8)
PC[0..7]
PD[0..7]
PE[0..7]
PF[0..7]
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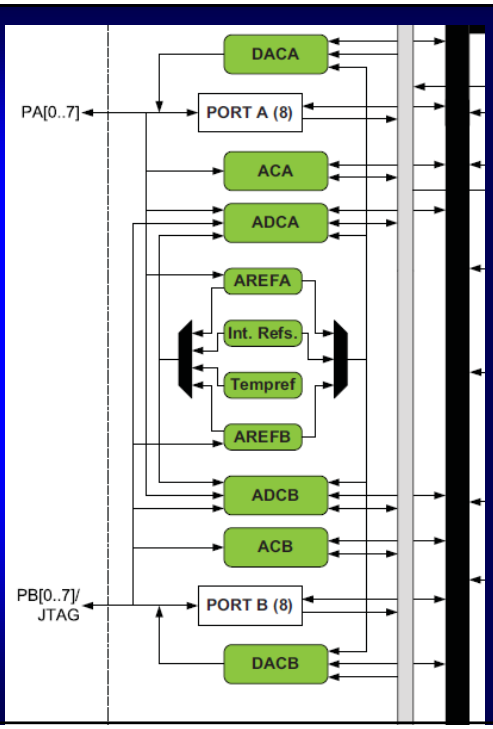
EEL 4744C: µP Apps

XMEGA Block Diagram

See doc8331 Fig 2-1



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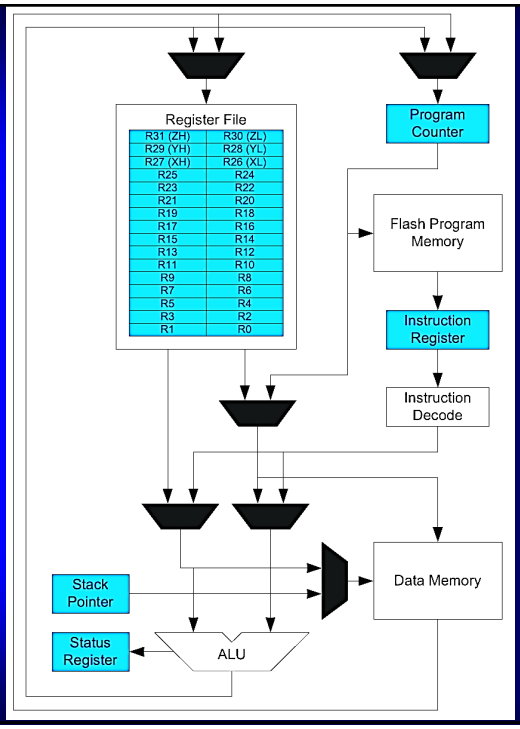
EEL 4744C: µP Apps

Conceptual XMEGA CPU Block Diagram

See doc8331 Fig 3-1



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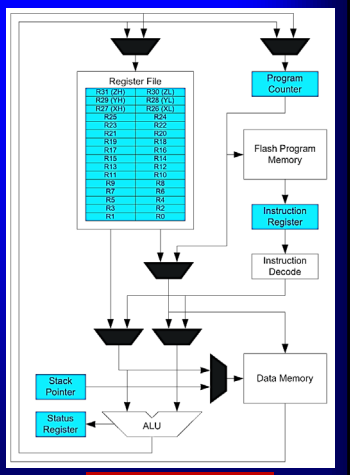
XMEGA Accumulator

- All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU)
  - > This allows **two independent registers** to be accessed in **one single instruction**, and executed in **one clock cycle**.
- Resulting architecture is more code efficient and faster than conventional single-accumulator or CISC based microcontrollers



See doc8331 Fig 3-1

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XMEGA is Little Endian

- When 32-bit values are saved the least significant 16 bits are saved first, in the lower address (and the most significant 16 bits are saved to the next higher address), i.e., XMEGA is a **little endian** processor
- Loading a single byte of the address register will always update the LSB byte while the MSB bytes are left unchanged
  - > See example

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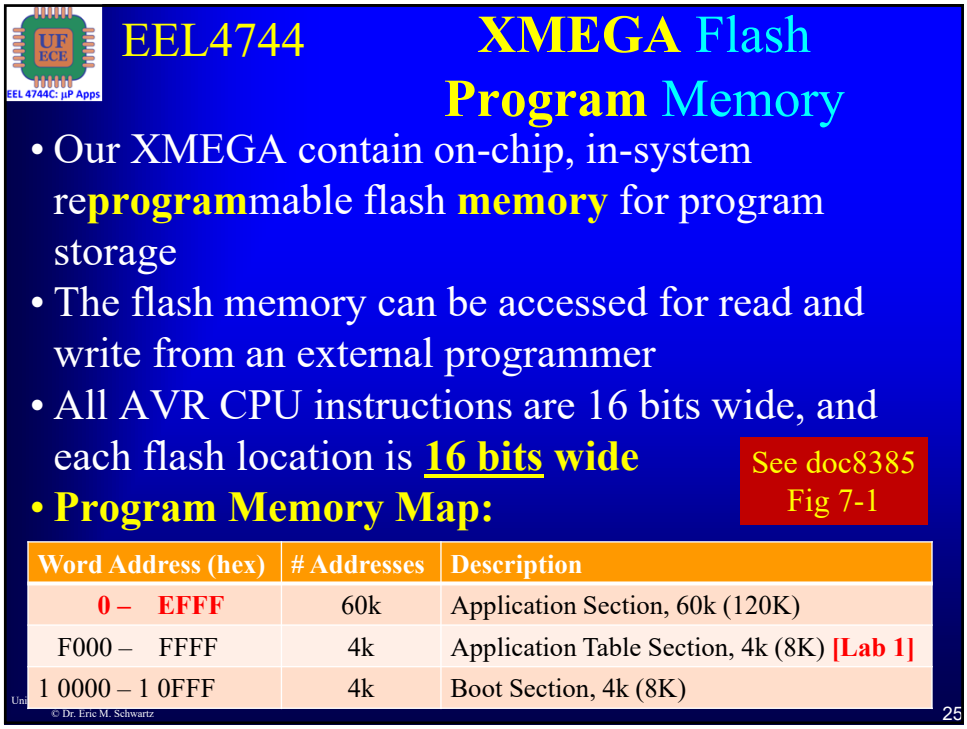
EEL4744
XMEGA Flash Program Memory
• Our XMEGA contain on-chip, in-system reprogrammable flash memory for program storage
• The flash memory can be accessed for read and write from an external programmer
• All AVR CPU instructions are 16 bits wide, and each flash location is 16 bits wide
• Program Memory Map:
See doc8385 Fig 7-1
Word Address (hex) | # Addresses | Description
0 – EFFF | 60k | Application Section, 60k (120K)
F000 – FFFF | 4k | Application Table Section, 4k (8K) [Lab 1]
1 0000 – 1 0FFF | 4k | Boot Section, 4k (8K)
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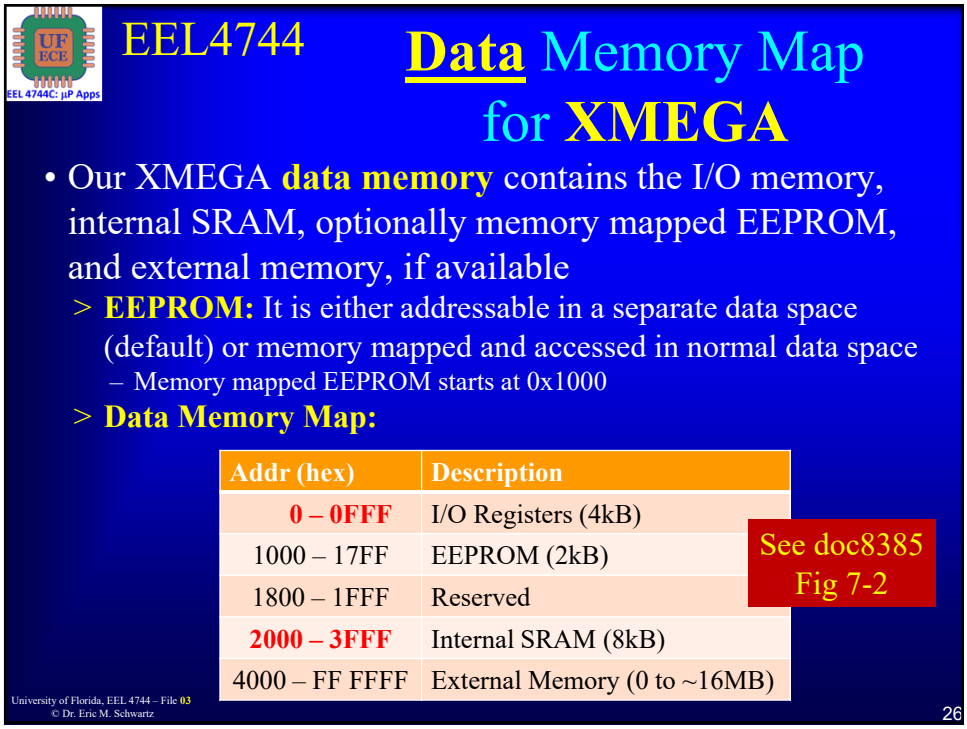
EEL4744
Data Memory Map for XMEGA
• Our XMEGA data memory contains the I/O memory, internal SRAM, optionally memory mapped EEPROM, and external memory, if available
> EEPROM: It is either addressable in a separate data space (default) or memory mapped and accessed in normal data space
– Memory mapped EEPROM starts at 0x1000
> Data Memory Map:
Addr (hex) | Description
0 – 0FFF | I/O Registers (4kB)
1000 – 17FF | EEPROM (2kB)
1800 – 1FFF | Reserved
2000 – 3FFF | Internal SRAM (8kB)
4000 – FF FFFF | External Memory (0 to ~16MB)
See doc8385 Fig 7-2
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See doc8385
Section 7.5-7.8

Data Memory Map for XMEGA

- **I/O Memory:** The status & configuration registers for peripherals and modules, including the CPU, are addressable through I/O memory locations
  - All I/O locations can be accessed by the load (**LD/LDS/LDD**) and store (**ST/STS/STD**) instructions, which are used to transfer data between the **32 registers** in the register file and the I/O memory
  - The **IN** and **OUT** instructions can address I/O memory locations in the range **0x00 - 0x3F** directly (**GPIO**, **VPORT0-3**, **CPU**)
- **General Purpose I/O Registers:** The lowest 16 I/O memory addresses (**R0-R15**) are reserved as general purpose I/O registers
  - These registers can be used for storing global variables and flags, as they are directly bit-accessible using the SBI, CBI, SBIS, and SBIC instructions
- **External Memory:** Four ports can be used for external memory, supporting external SRAM, SDRAM, and memory mapped peripherals such as LCD displays (see "EBI – External Bus Interface" in section 28)

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Shared address/data bus

- Many µC's and µP's (especially older ones) have shared address and data bus
  - Many that do not have a shared bus option do **NOT** have external busses at all!
  - 68HC11 uses 8-pins, AD7-0 for 8-bits of data and 8-bits of address
  - For the 68HC12, you must latch all 16-pins of the address/data bus, even if you are only using 8-bits of data

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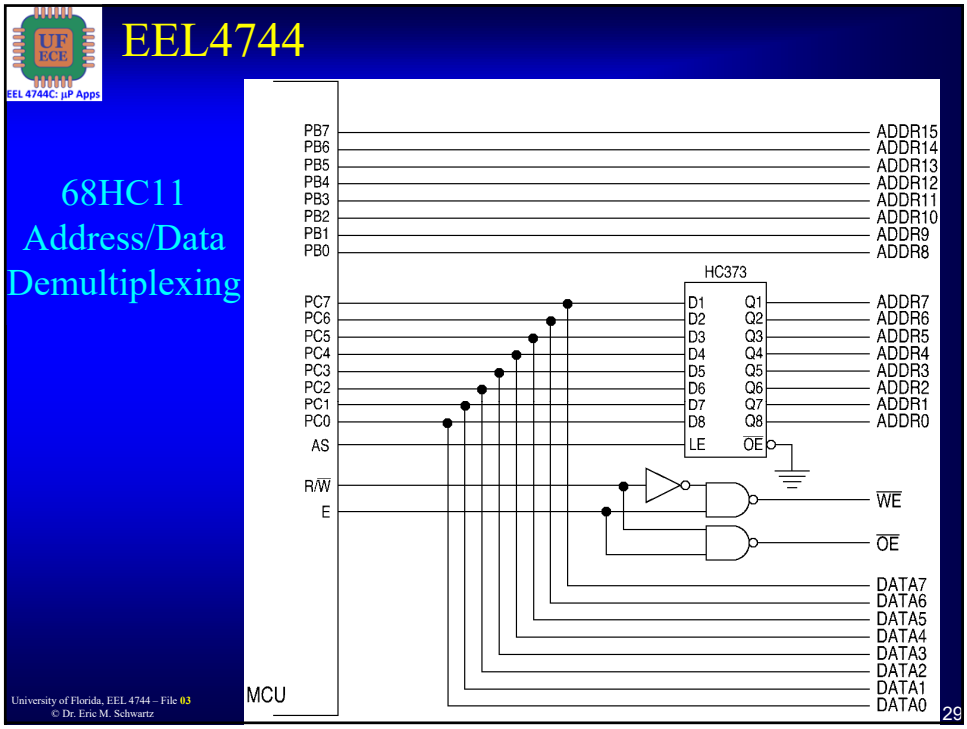
EEL4744
EEL 4744C: µP Apps
68HC11
Address/Data
Demultiplexing
PB7
PB6
PB5
PB4
PB3
PB2
PB1
PB0
ADDR15
ADDR14
ADDR13
ADDR12
ADDR11
ADDR10
ADDR9
ADDR8
HC373
PC7
PC6
PC5
PC4
PC3
PC2
PC1
PC0
AS
R/W
E
D1
D2
D3
D4
D5
D6
D7
D8
LE
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
OE
ADDR7
ADDR6
ADDR5
ADDR4
ADDR3
ADDR2
ADDR1
ADDR0
WE
OE
DATA7
DATA6
DATA5
DATA4
DATA3
DATA2
DATA1
DATA0
MCU
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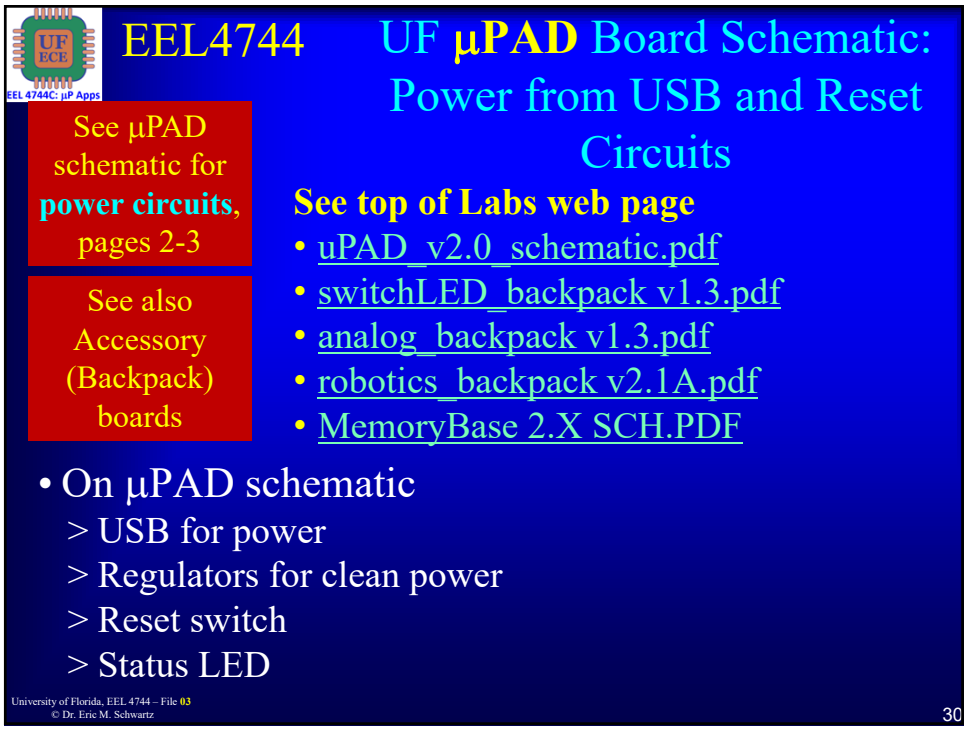
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EEL 4744C: µP Apps
UF µPAD Board Schematic:
Power from USB and Reset Circuits
See µPAD schematic for power circuits, pages 2-3
See also Accessory (Backpack) boards
See top of Labs web page
• uPAD_v2.0_schematic.pdf
• switchLED_backpack v1.3.pdf
• analog_backpack v1.3.pdf
• robotics_backpack v2.1A.pdf
• MemoryBase 2.X SCH.PDF
• On µPAD schematic
> USB for power
> Regulators for clean power
> Reset switch
> Status LED
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